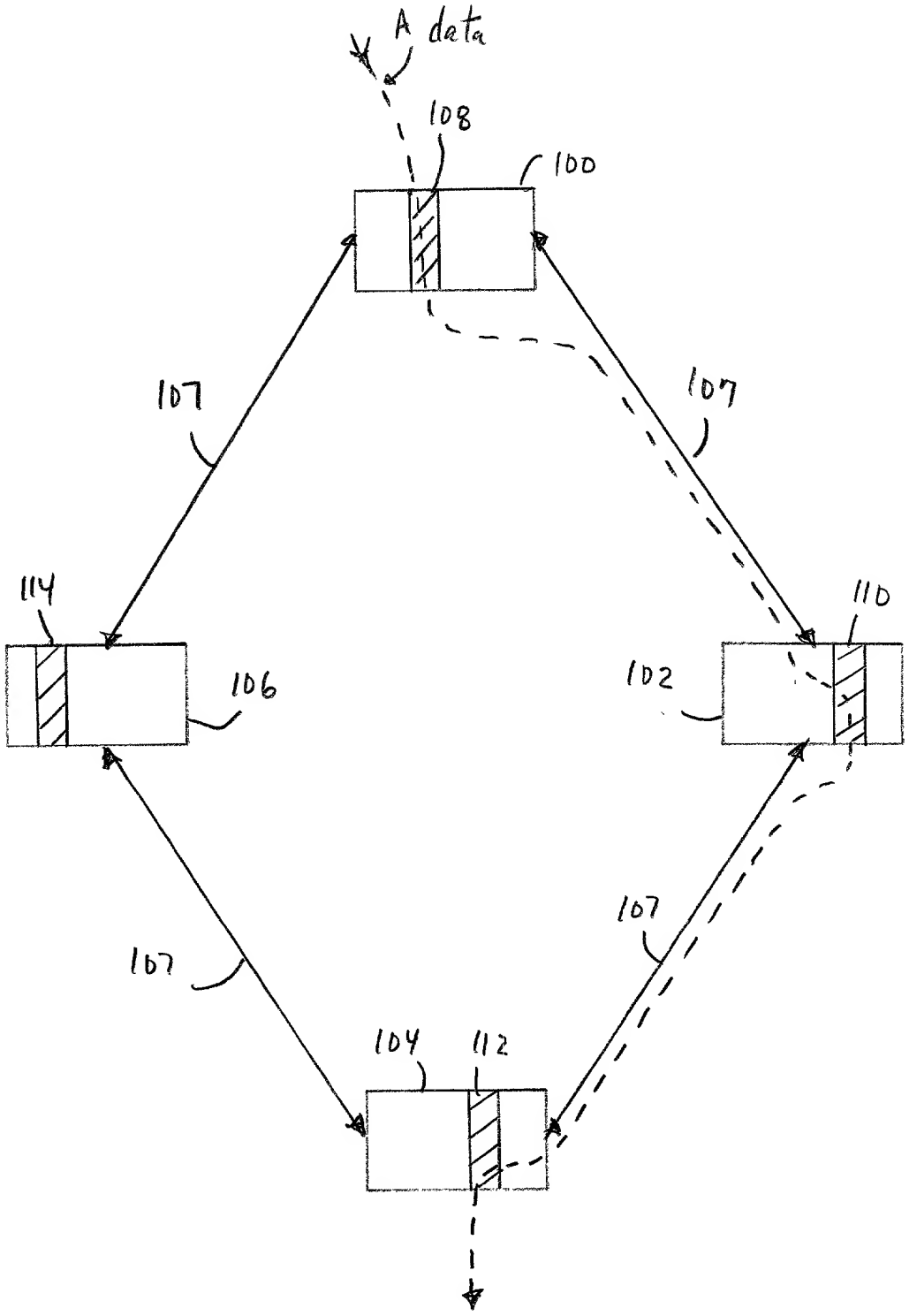

FIG. 1

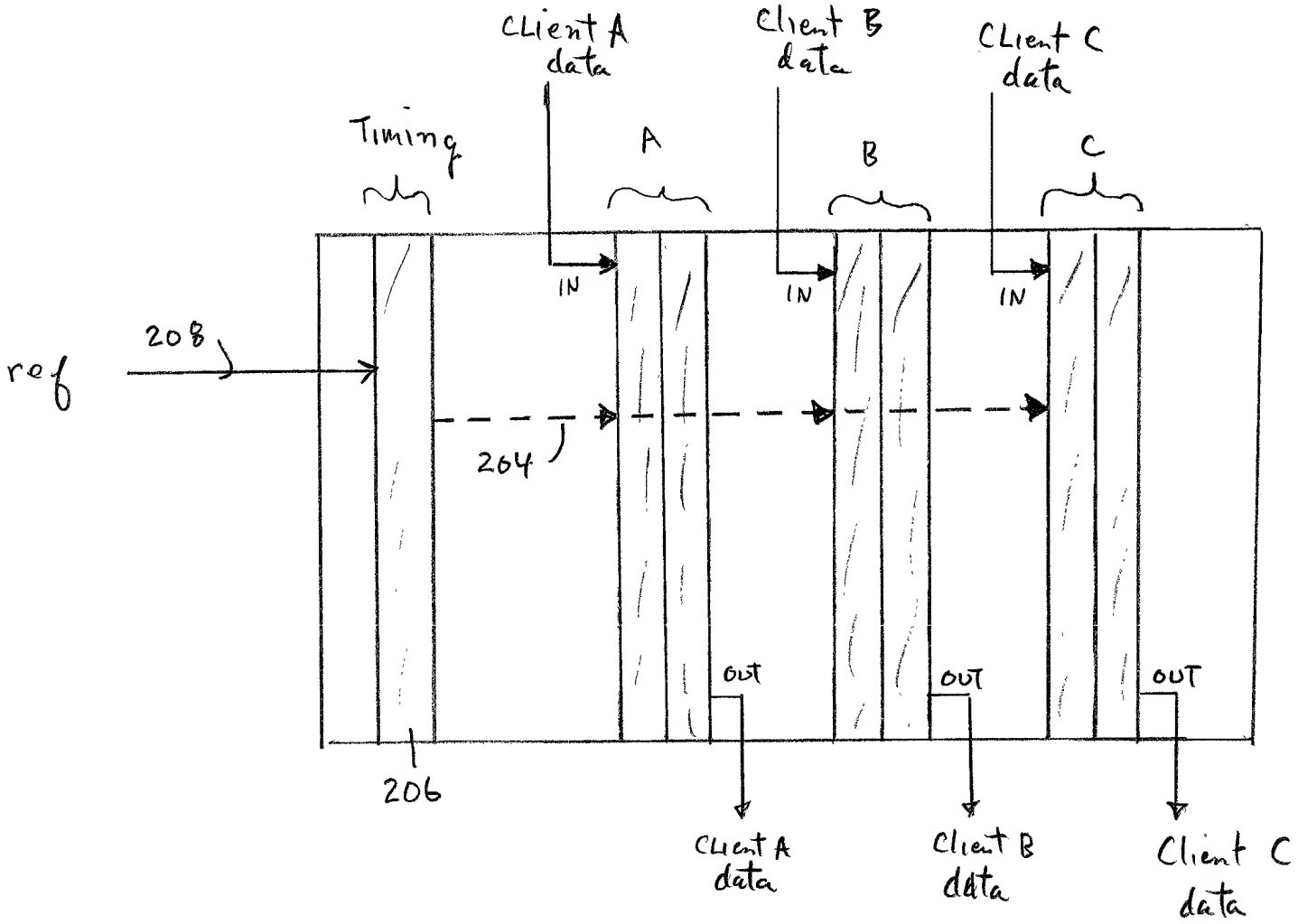
Client A data
Client B data
Client C data
Timing
A
B
C
IN
IN
IN
ref
208
264
OUT
OUT
OUT
206
Client A data
Client B data
Client C data

FIG. 2

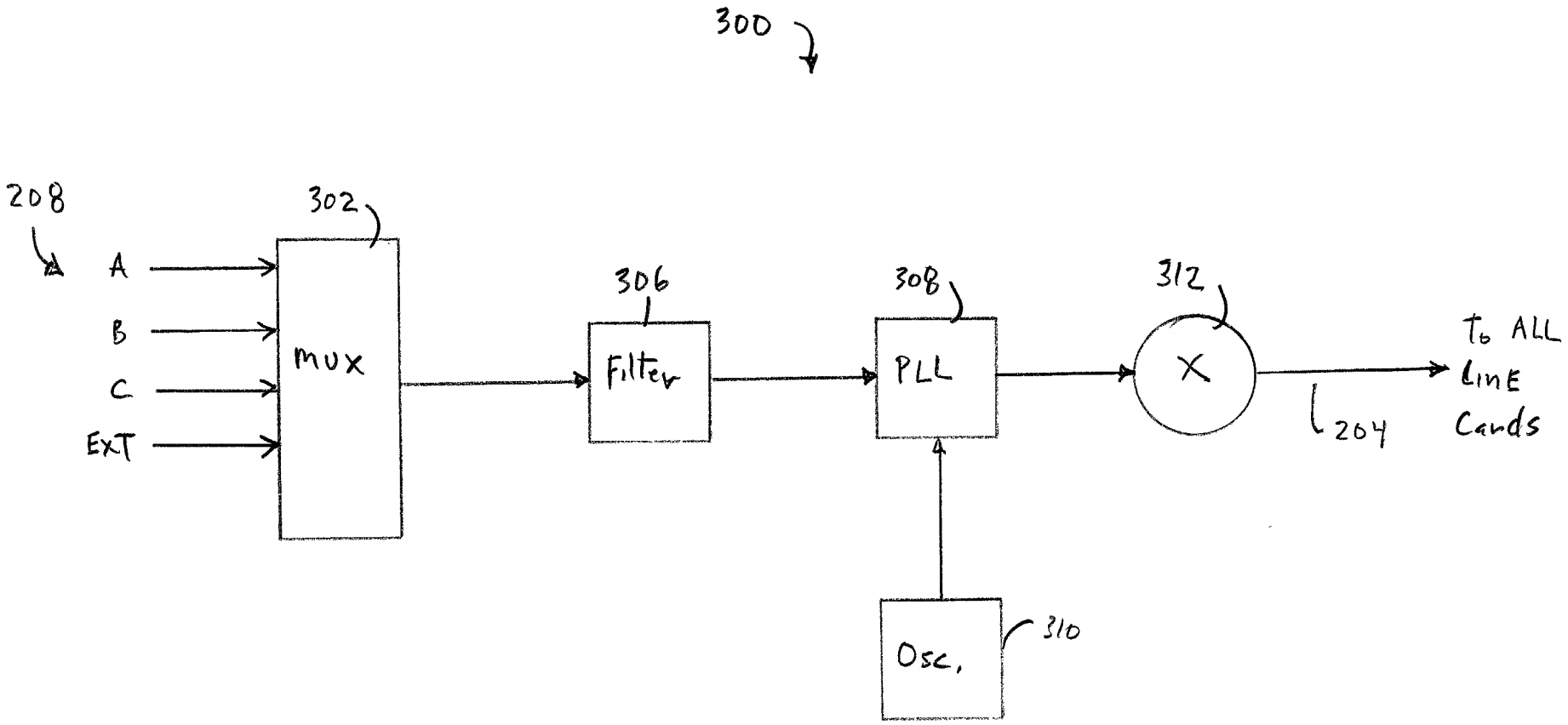
300
208
302
A
B
C
EXT
MUX
306
Filter
308
PLL
312
X
To ALL
Line
Cards
204
Osc.
310

FIG. 3

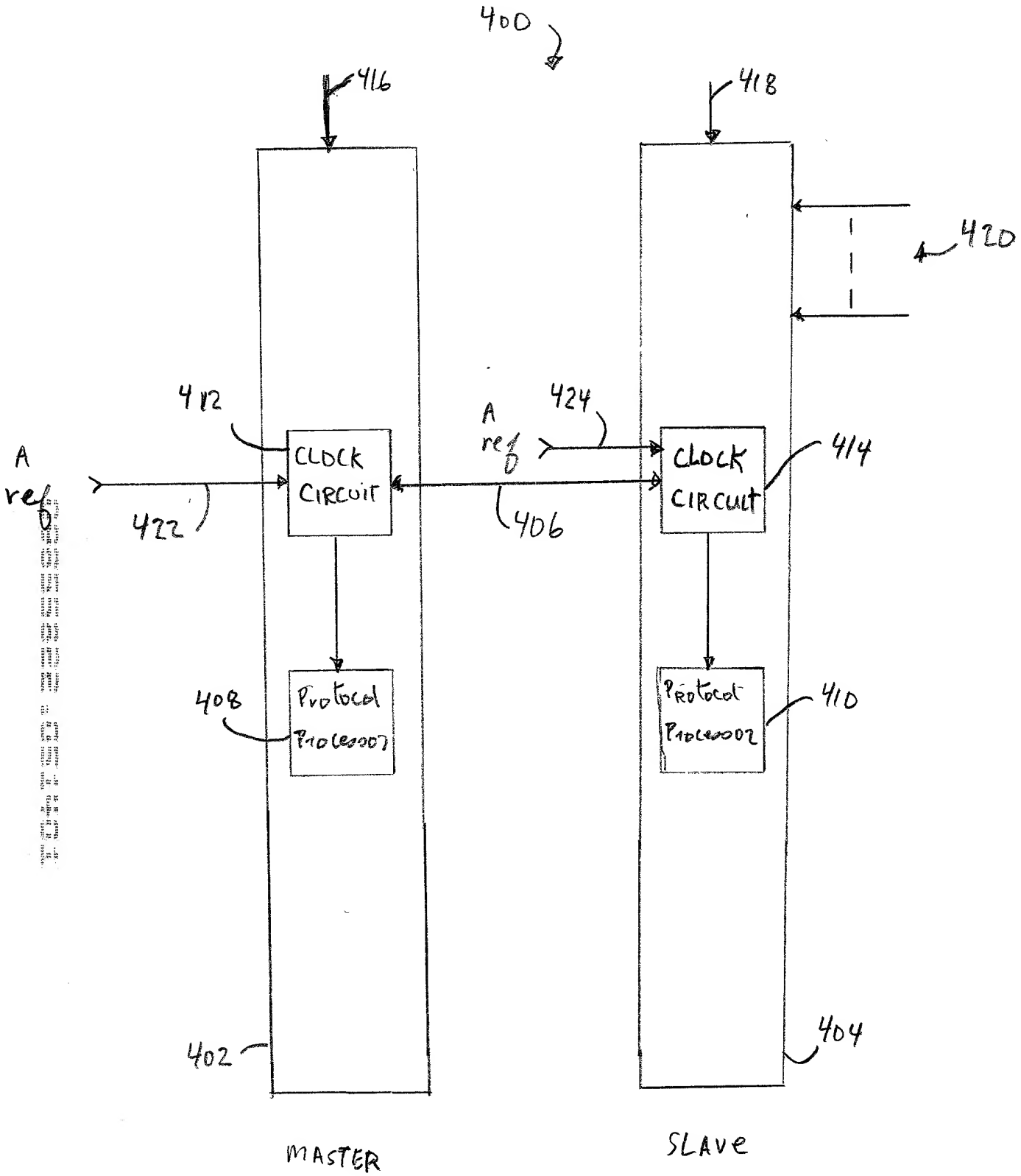
400
416
418
420
412
424
A ref 0
CLOCK CIRCUIT
CLOCK CIRCUIT
414
422
406
408
PROTOCOL PROCESSOR
PROTOCOL PROCESSOR
410
402
404
MASTER
SLAVE

FIG. 4

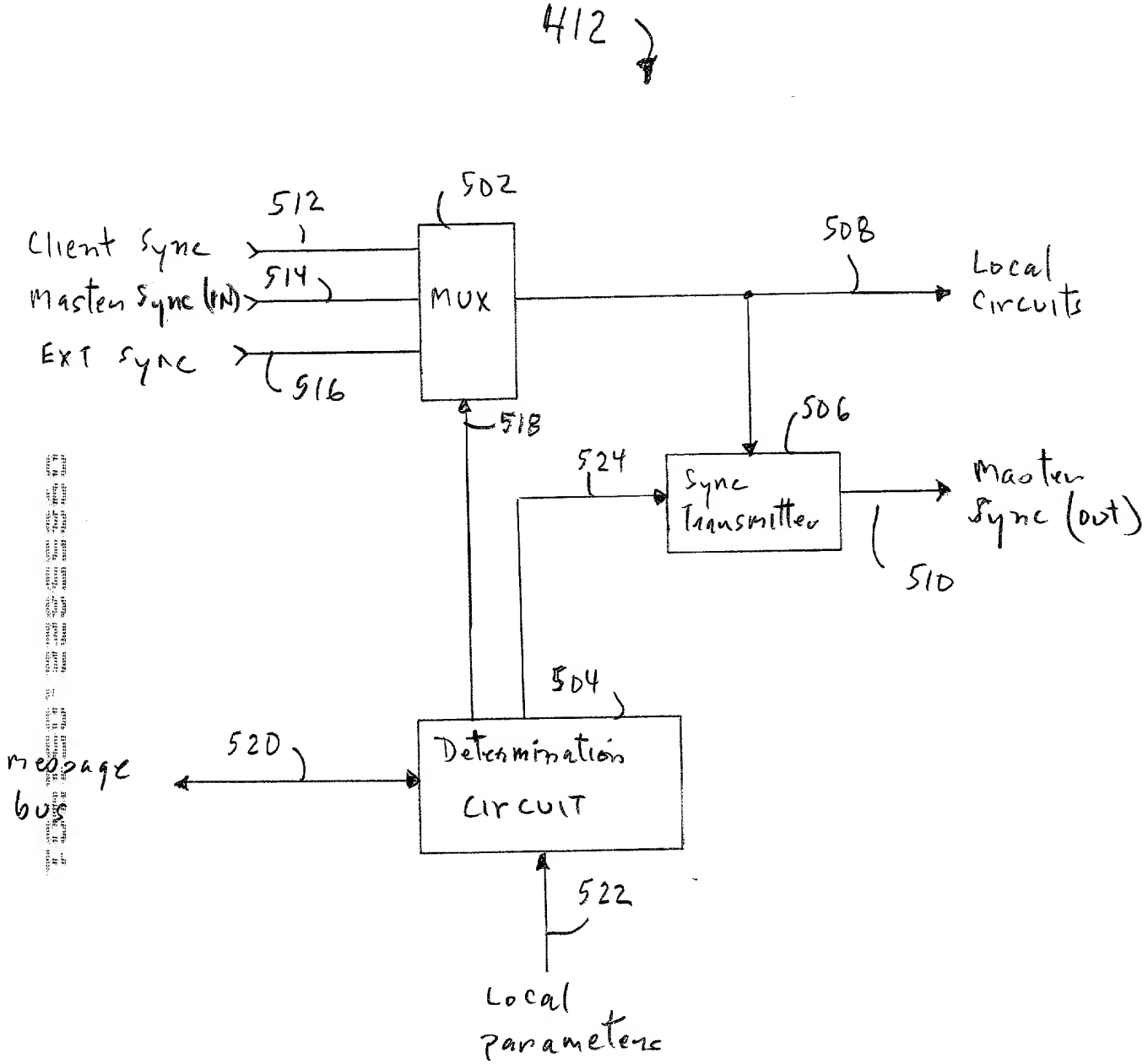
412
502
512
Client Sync
514
Master Sync (IN)
EXT Sync
516
MUX
508
Local Circuits
518
506
524
Sync Transmitter
Master Sync (out)
510
504
520
message bus
Determination Circuit
522
Local parameters

FIG. 5

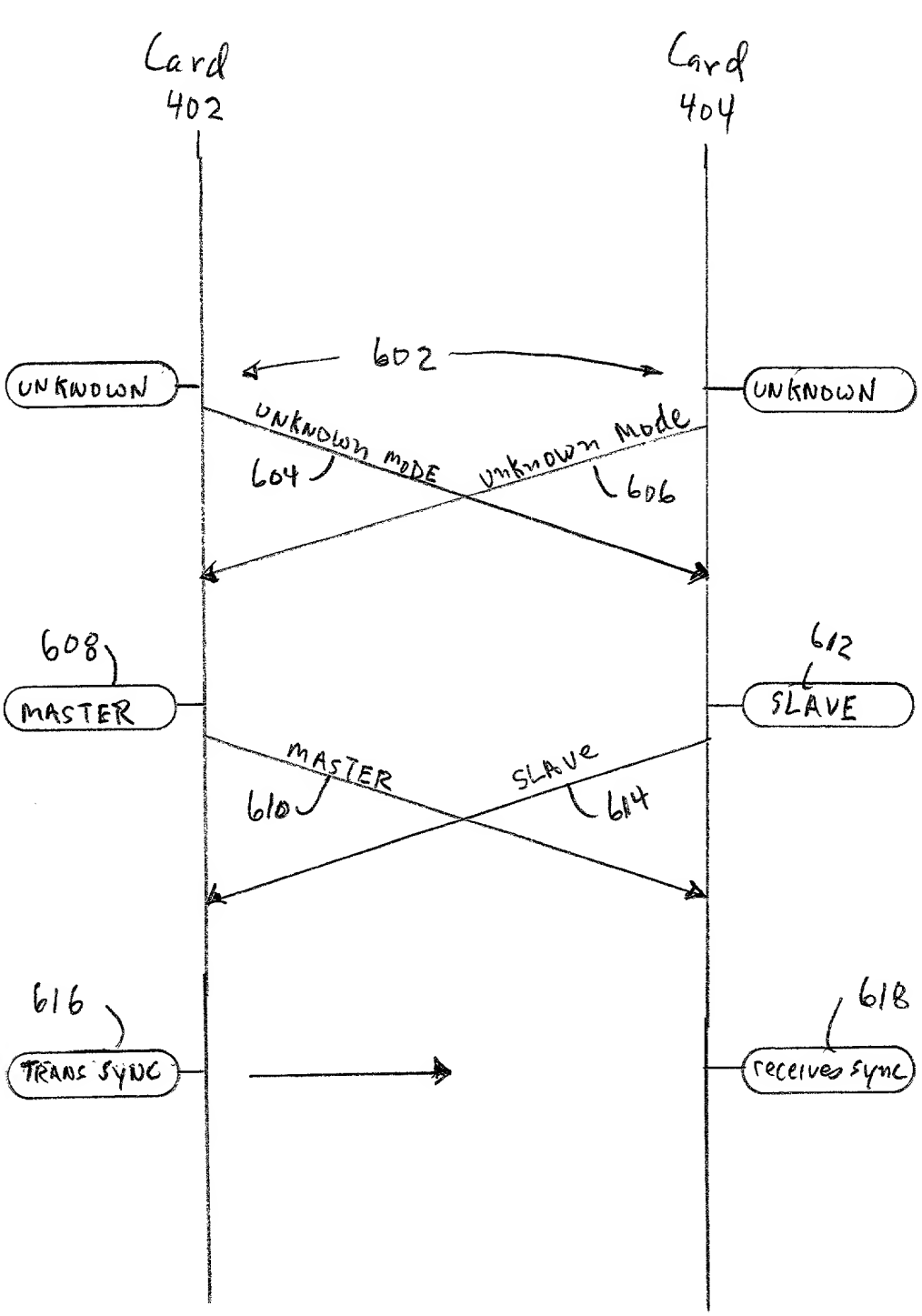
600
Card 402
Card 404
602
UNKNOWN
UNKNOWN
UNKNOWN MODE
604
Unknown Mode
606
608
MASTER
612
SLAVE
MASTER
610
SLAVE
614
616
TRANS SYNC
618
receives sync

FIG. 6